A Novel DC Voltage Control Method for STATCOM Based on Hybrid Multilevel H-Bridge Converter  
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Abstract—This paper presents a transformerless static synchronous compensator (STATCOM) system based on hybrid multilevel H-bridge converter with delta configuration. This hybrid multilevel STATCOM is characterized by per-phase series connection of a high-voltage H-bridge converter operating at fundamental frequency and a low-voltage H-bridge converter operating at 5 kHz without any other circuit for dc voltage control. A new control strategy is proposed in this paper with focus on dc voltage regulation. Clustered balancing control is realized by injecting a zero-sequence current to the delta-loop, while individual voltage control is achieved by adjusting the fundamental content of ac quasi-square-waveform voltage of high-voltage converter. A downscaled experimental prototype rated at 100 V and 3 kVA is constructed in author’s laboratory. Experimental results show that the hybrid multilevel STATCOM performs satisfactory not only improving efficiency and waveform quality, but also compensating reactive power and negative-sequence current while maintaining dc voltage at the given value.

Index Terms—Cascade H-bridge, dc voltage control, hybrid multilevel, static synchronous compensator (STATCOM).

I. INTRODUCTION

A CASCADED H-bridge converter with equal dc voltage has been widely used for static synchronous compensator (STATCOM) application because of natural modular and high-quality output spectrum [1]–[7], [25]. Compared with diode-clamped converter and flying capacitor converter, the cascaded single-phase H-bridge converter saves a large amount of clamped diodes and flying capacitors [8]. However, further improvement of power efficiency and waveform quality is expected of cascade H-bridge topology in high-power application [9]. Traditionally, low-distorted ac voltage waveform is achieved by either increasing switching frequency or increasing the cascaded number of modules, which bring high power loss or high cost to the STATCOM system. Fortunately, hybrid multilevel technology provides a good tradeoff between waveform quality and switching loss [9]. The important advantages of hybrid multilevel converters are as follows: increasing voltage levels of output waveform, improving ac current quality, reducing switching frequency resulting in low switching loss, as well as enhancing converter efficiency.

As the concept of “hybrid multilevel” was proposed in the literature [10], great attentions have been paid to this field. In order to achieve hybrid multilevel, many approaches have been published in the literature [11]–[22], [26], [27]. A hybrid topology with the series connection of three-phase full-bridge converter (two- or three-level) and single-phase H-bridge converter is adopted in the literature [11]–[16], [26], [27]. This topology effectively produces higher voltage levels compared with traditional ones with the same number of switches, but it is companied by a problem of dc voltage control. One popular method for capacitor voltage control is selecting switching states redundancy [11]–[13], which introduces another problem of uncertain switching frequency for relevant devices. To avoid the issue of dc voltage control, dc link of the hybrid topology is connected directly to expensive dc supplies such as battery, fuel cell, and rectifier [14], [15], [26]. In [16], a three-phase three-level converter is fed by rectifiers, while the H-bridge converter uses a capacitor as a replacement of dc source for cost saving. Capacitor voltage and neutral point clamped voltage is regulated by adjusting common-mode voltage. This control algorithm requires a large amount of real-time online calculation, which brings difficulty for STATCOM application. In [27], all the dc-link voltages are controlled purely by control algorithm. Reactive-power regulation is realized by adjusting dc voltages. However, this control method is based on steady-state model and the dynamic performance is not discussed. Additionally, the capability of compensating unbalanced load is not mentioned either.

Moreover, hybrid multilevel topology based on cascaded single-phase H-bridge converter with unequal dc voltage is considered in [17]–[22]. The literature [17], [18] describes a motor drive system based on hybrid multilevel H-bridge converters with unequal dc voltage supplies. The mentioned control method is not suitable for STATCOM system because the dc sources are replaced by capacitors in the STATCOM system. The literature [19]–[21] provides new solution with a high-voltage converter fed by dc supplies and a low-voltage converter fed by dc capacitor. In [19], a diode-clamped H-bridge with multioutput boost rectifier functions as the high-voltage inverter. The utilization of clamped diode and rectifier increases the cost of whole system. In [20], dc voltage ratio of 4:2:1 is arranged to the series-connected H-bridge converters. The expensive isolated dc supplies are required for ratio-4 and ratio-2 converters. Fundamental frequency modulation is adopted in the literature [21] for cascade hybrid H-bridge converters. In [21], the selective harmonic elimination method is adopted for hybrid modulation and selecting switching redundant states is applied for

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capacitor voltage control. The quality of output voltage waveform is not good, which prevents this method for STATCOM application. The literature [22] proposes an active power filter system composed of three series-connected H-bridge converters with voltage ratio of 6:2:1.5, which is realized by control algorithm. However, dc voltage control strategy is not discussed in detail and three-phase performance is not verified by experiments.

Recently, some other interesting topologies have been published in [28]–[30]. In [28], a hybrid-source impedance network with the dc link of series-connected z-sources is presented for enhancing the three-phase ac voltage levels, but it is not suitable for STATCOM application because of the utilization of large amount of dc sources. The literature [29] describes a multi-level circuit topology based on switched-capacitors and diode-clamped converters. The model related to switched-capacitor converters is given in the literature [30]. This kind of converters can successfully produce high-voltage levels and the issue with dc voltage balancing can be easily solved by choosing proper switching sequences. This structure requires a plenty of switching devices, so it have not widely been accepted in medium-voltage application.

In this paper, the authors focused on the STATCOM application using hybrid multilevel converters. The delta-type cascaded hybrid single-phase H-bridge topology is preferred because of modularity and simplicity. This paper proposed a new dc voltage control strategy for those hybrid multilevel converters. Clustered balancing control is achieved by injecting zero-sequence current to the delta-loop, and the individual voltage control is realized by trimming the fundamental content of quasi-square-wave voltage of high-voltage converters. Compared with other hybrid multilevel approaches, this control strategy along with the STATCOM system has the advantages of fast-speed response to load change, accurate unbalanced load compensation, no auxiliary circuit for dc links, less on-line calculation, specific unequal dc voltage regulation, as well as certain but unequal switching frequencies. The experiment results obtained from the downscaled prototype confirm the merits.

II. CONFIGURATION OF THE 100-V 3-KVA STATCOM SYSTEM

Fig. 1 shows the configuration of a three-phase STATCOM rated at 100 V and 3 kVA, which is based on hybrid cascade single-phase H-bridge cells. Table I summarizes the circuit parameters. The cascade number of \( N = 2 \) is assigned to the prototype because of the restriction of the author’s laboratory condition, resulting in six converter cells in total. In each phase cluster, one single-phase H-bridge cell is controlled as a high-voltage converter with dc-link voltage of 110 V, and the other single-phase H-bridge cell acts as a low-voltage converter with dc-link voltage of 65 V. The explanation of this arrangement is described in the next section. Each cell is equipped with an isolating electrolytic capacitor with a capacitance value of 9400 \( \mu \)F. No auxiliary circuit is connected to the six split dc capacitors except for six voltage sensors. An ac inductor is also required for each cluster to support the difference between the sinusoidal source voltage and the ac pulsewidth modulation (PWM) voltage of cluster, and it also makes contribution in filtering out switch ripples caused by high-frequency modulation.

In experiment, switching frequencies of 50 Hz and 5 kHz are assigned to high-voltage converter and low-voltage converter, respectively. The constant dc voltages are achieved purely by the control algorithm. This design is reasonable to verify the

<table>
<thead>
<tr>
<th>Table I: Circuit Parameters in Fig. 1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Nominal line-to-line rms voltage</strong></td>
</tr>
<tr>
<td><strong>Power rating</strong></td>
</tr>
<tr>
<td><strong>AC inductor</strong></td>
</tr>
<tr>
<td><strong>Starting resistor</strong></td>
</tr>
<tr>
<td><strong>Back ground inductance</strong></td>
</tr>
<tr>
<td><strong>DC voltage for cell u1,v1,w1</strong></td>
</tr>
<tr>
<td><strong>DC voltage for cell u2,v2,w2</strong></td>
</tr>
<tr>
<td><strong>DC capacitor</strong></td>
</tr>
<tr>
<td><strong>Switching frequency for cell u1,v1,w1</strong></td>
</tr>
<tr>
<td><strong>PWM carrier frequency for cell u2,v2,w2</strong></td>
</tr>
</tbody>
</table>
improvement of output voltage waveform and the performance of the 100-V 3-kVA STATCOM system, because these special characteristics mainly relay on control strategy.

As shown in Fig. 2, this experimental system is totally controlled by a fully digital controller using a 32-bit digital signal processor (DSP) and field-programmable gate arrays (FPGA). Most of the calculation is dealt with by the DSP chip and the hybrid modulation strategy is implemented on FPGA chip. The gating signals for all the switching devices are generated by the hybrid modulation, which matches the 10-kHz sample frequency well.

Hybrid modulation shown in Fig. 3 includes two parts: fundamental modulation and PWM modulation. The fundamental modulation could simply be described as follows: when the sinusoidal command is higher than a threshold value of $V_{\text{cmp}}$, the high-voltage converter outputs positive voltage; as the sinusoidal command is lower than the negative threshold value of $-V_{\text{cmp}}$, the high-voltage converter outputs negative voltage; and if the sinusoidal command is in the range between $-V_{\text{cmp}}$ and $V_{\text{cmp}}$, the high-voltage converter outputs zero. The remaining part of sinusoidal command and the quasi-square-waveform voltage is the command voltage for low-voltage converter. It is modulated by single-polar PWM modulation technology with the carrier frequency of 5 kHz. Based on this modulation strategy, an ac waveform with higher voltage levels is produced. It brings the advantages of improving output quality, keeping high equivalent switching frequency, and reducing power loss.

III. MATHEMATICAL ANALYSIS OF CAPACITOR VOLTAGE CONTROL

A. Fundamentals of Circuit Operation

In each cluster, the high-voltage converter outputs quasi-square waveform, while the low-voltage converter outputs the remaining part between sinusoidal command and the quasi-square waveform shown in Fig. 4. Therefore, low-frequency contents in total ac voltage are completely eliminated. The total ac voltage only includes fundamental component and harmonic components around switching frequency. Three-phase smooth sinusoidal currents are guaranteed because the high-frequency components can be easily filtered by interface inductors. The sharp change of load can be well followed by dynamically trimming the sinusoidal command voltage, which ensures the fast-speed response.

As the issue with dc voltage control is also very crucial for safe operation. DC voltage control strategy is also investigated in this paper. As shown in Fig. 4, a fundamental-frequency zero-sequence current is suggested to the delta-loop for balancing of dc voltages among three phases. This clustered balancing method enables the STATCOM system to compensate unbalanced load. Moreover, unequal dc voltages of high-voltage converter and low-voltage converter are achieved by the effect
of individual voltage control, which suggests a small trim to the fundamental contents of quasi-square-waveform voltage of high-voltage converter for active-power redistribution between high-voltage and low-voltage converters. In the whole process, the low-voltage converter always compensates the remaining part to match the sinusoidal command. Additionally, the sum of all capacitor voltages is regulated by the algorithm of overall voltage control.

B. Injection of Zero-Sequence Current for Clustered Balancing Control

The command zero-sequence current with the symbols of \( I_o \) and \( \varphi_o \) could be written as

\[
i_o = I_o \sin(\omega t + \varphi_o)
\]  

(1)

where \( I_o \) and \( \varphi_o \) are the magnitude and original phase angle, respectively. The average power redistributed by zero-sequence current is expressed as

\[
\begin{align*}
\bar{p}_{oab} &= \frac{1}{T_s} \int_{t}^{t+T_s} v_{oab} \cdot i_o \, dt = \frac{V_s I_o}{2} \cos(\varphi_o) \\
\bar{p}_{obc} &= \frac{1}{T_s} \int_{t}^{t+T_s} v_{obc} \cdot i_o \, dt = \frac{V_s I_o}{2} \cos \left( \varphi_o + \frac{2\pi}{3} \right) \\
\bar{p}_{oca} &= \frac{1}{T_s} \int_{t}^{t+T_s} v_{oca} \cdot i_o \, dt = \frac{V_s I_o}{2} \cos \left( \varphi_o - \frac{2\pi}{3} \right)
\end{align*}
\]  

(2)

where \( V_s \) is the magnitude of line-to-line grid voltage and \( T_s \) is a line period. \( v_{oab}, v_{obc}, \) and \( v_{oca} \) are the three-phase line-to-line voltages. The sum of the three equations in (2) is equal to zero, which indicates that zero-sequence current just causes the redistribution of active power among three clusters without any influence on total active power. The redistributed power could be used for canceling that is caused by unbalanced compensating current, as well as for providing proper amount of power for balancing of dc voltages among three clusters. Therefore, the average power could be expressed as

\[
\begin{align*}
\bar{p}_{oab} &= \bar{p}_{oab} + \Delta \bar{p}_{oab} \\
\bar{p}_{obc} &= \bar{p}_{obc} + \Delta \bar{p}_{obc} \\
\bar{p}_{oca} &= \bar{p}_{oca} + \Delta \bar{p}_{oca}
\end{align*}
\]  

(3)

where terms of \( \bar{p}_{oab}, \bar{p}_{obc}, \) and \( \bar{p}_{oca} \) are used for power cancellation and terms of \( \Delta \bar{p}_{oab}, \Delta \bar{p}_{obc}, \) and \( \Delta \bar{p}_{oca} \) are used for balancing of dc voltages among clusters. For simplification, the clustered balancing control considers a cluster of series-connected converters as one equivalent single-phase H-bridge converter. The mathematical relationship between the clustered capacitor voltage and active power is calculated by

\[
\Delta p_{ab} = C \cdot V_{cu} \frac{dv_{cu}}{dt} + \frac{2}{R_c} V_{cu} v_{cu}
\]  

(4)

where \( R_c \) is the equivalent parallel resistance of u-phase cluster, which represents the power loss of u-phase converters. Equation (5) gives the transfer function, which is obtained by applying Laplace transformation to (4). According to the following equation, the regulator for clustered balancing control could be designed:

\[
G_{vp} = \frac{v_{cu}}{\Delta p_{ab}} = \frac{R}{R C V_{cu} s + 2 V_{cu}}.
\]  

(5)

In practice, the amount of active power redistributed by zero-sequence current is calculated by closed-loop-based regulator. Once the required power is determined, the command zero-sequence current can be obtained by solving (2). The magnitude \( I_o \) and original phase angle \( \varphi_o \) are derived by

\[
\begin{align*}
I_o &= \frac{2}{\sqrt{3}} \sqrt{(\bar{p}_{oab})^2 + \frac{1}{3}(\bar{p}_{oab} + 2 \bar{p}_{obc})^2} \\
\varphi_o &= \tan^{-1} \left( -\frac{1}{\sqrt{3}} \left( 1 + \frac{2 \bar{p}_{obc}}{\bar{p}_{oab}} \right) \right).
\end{align*}
\]  

(6)

C. Trimming Fundamental Content of Quasi-Square Waveform for Individual Voltage Control

As the clustered dc voltage is controlled and maintained, the individual control becomes necessary because of the different power loss between high-voltage converter and low-voltage converter. Due to the symmetry of structure and parameters among the three phases, u-phase cluster was taken as an example for individual control analysis.

As shown in Fig. 5, the fundamental voltage and input current of u-phase cluster could be assumed as

\[
v_{iu} = V_{iu} \sin(\omega t - \varphi_{iu})
\]  

(7)

\[
i_{cu} = I_c \cos(\omega t - \varphi_{cu})
\]  

(8)
During one line period, the average power absorbed by the high-voltage converter could be calculated as

\[
\overline{p_{iu1}} = \frac{1}{T_s} \left( \int_{\frac{\varphi_{iu} + \pi/2}{2} - W_u/2}^{\frac{\varphi_{iu} + \pi/2}{2} + W_u/2} V_{cu1} \cdot i_{cu} \, dt \right.
\]

\[
+ \left. \int_{\frac{\varphi_{iu} + 3\pi/2}{2} - W_u/2}^{\frac{\varphi_{iu} + 3\pi/2}{2} + W_u/2} V_{cu1} \cdot i_{cu} \, dt \right)
\]

\[
= \frac{2}{\pi} V_{cu1} \cdot I_c \cdot \sin(\varphi_{cu} - \varphi_{iu}) \sin \left( \frac{W_u}{2} \right)
\]  

(9)

where \(V_{cu1}\) is the high-voltage dc link; \(I_c\) is the magnitude of input current; \(\varphi_{cu}\) is the original phase angle referring to the pure reactive current, which is introduced to represent the active power absorbed by high-voltage converter; \(\varphi_{iu}\) is also a original phase angle respecting to the source voltage; and \(W_u\) is the pulselength of the quasi-square-waveform voltage of high-voltage converter. Equation (9) implies that the active power of high-voltage converter is affected by \(V_{cu1}, I_c, \varphi_{cu}, \varphi_{iu}\), and \(W_u\). Actually, \(I_c\) and \(\varphi_{cu}\) are decided by the reference current. Therefore, \(\varphi_{iu}\) and \(W_u\) are the only factors that could be used for adjusting dc voltage of high-voltage converter. In this paper, the adjustment of both \(\varphi_{iu}\) and \(W_u\) is preferred, which is realized by trimming the modulated waveform along the direction of input current \(i_{cu}\).

As shown in Fig. 5, the mathematical relationship between threshold value \(V_{cmp}\) and pulselength \(W_u\) could be expressed as

\[
\begin{align}
V_{iu}\sin(\omega t_0 - \varphi_{iu}) &= V_{cmp} \\
\frac{\pi}{2} + \varphi_{iu} - \omega t_0 &= \frac{W_u}{2}.
\end{align}
\]

(10)

By solving (10), the result is obtained by

\[
\sin \left( \frac{W_u}{2} \right) = \left\{ \begin{array}{ll}
\frac{\sqrt{V_{iu}^2 - V_{cmp}^2}}{V_{iu}} & \text{if } V_{iu} \geq V_{cmp} \\
\frac{\sqrt{V_{iu}^2 - V_{cmp}^2}}{V_{iu}} & \text{if } V_{iu} < V_{cmp}\end{array} \right.
\]  

(11)

Substituting (11) into (9), the average power obtained by the high-voltage converter can be rewritten as

\[
\overline{p_{iu1}^{\prime}} = \frac{2}{\pi} V_{cu1} \cdot I_c \cdot \sin(\varphi_{cu} - \varphi_{iu}) \frac{\sqrt{V_{iu}^2 - V_{cmp}^2}}{V_{iu}}.
\]  

(12)

The average power calculated by the modulated waveform is expressed as

\[
\overline{p_{iu1}^{\prime}} = \frac{1}{T_s} \int_{t}^{t+T_s} (v_{iu} \cdot i_{cu}) \, dt = \frac{1}{2} V_{iu} \cdot I_c \cdot \sin(\varphi_{cu} - \varphi_{iu}).
\]

(13)

The relationship between the average power absorbed by the high-voltage converter and the power calculated by the modulated waveform is obtained by

\[
C_{\text{value}} = \frac{\overline{p_{iu1}^{\prime}}}{\overline{p_{iu1}}} = \frac{4}{\pi} V_{cu1} \frac{\sqrt{V_{iu}^2 - V_{cmp}^2}}{V_{iu}^2}.
\]  

(14)

According to (14), the average power absorbed by high-voltage converter could be easily obtained by calculating the modulated waveform. In order to control the capacitor voltage of high-voltage converter, the modulated waveform can be changed as

\[
v_{iu}^{\prime} = v_{iu} + \Delta e \cdot i_{cu} = V_{iu}\sin(\omega t - \varphi_{iu})
\]

\[
+ \Delta e \cdot I_c \cos(\omega t - \varphi_{cu})
\]

(15)

where \(\Delta e\) is the trimming amplitude along the direction of input current. The modulated waveforms before and after change are shown in Fig. 6. And then, the power calculated by the modulated waveform is obtained by

\[
\overline{p_{iu1}^{\prime}} = \frac{1}{T_s} \int_{t}^{t+T_s} (v_{iu}^{\prime} \cdot i_{cu}) \, dt = \overline{p_{iu1}} + \frac{1}{2} \Delta e \cdot I_c^2.
\]

(16)

Based on (14), the average power absorbed by high-voltage converter is rewritten as

\[
\overline{p_{iu1}^{\prime}} = C_{\text{value}} \cdot \overline{p_{iu1}} = \overline{p_{iu1}} + \frac{1}{2} \Delta e \cdot I_c^2 \cdot C_{\text{value}}.
\]

(17)

Therefore, the change of power for high-voltage converter could be obtained as

\[
\Delta p_{iu1} = \frac{2}{\pi} \frac{\Delta e}{L_c} \cdot V_{cu1} \frac{\sqrt{V_{iu}^2 - V_{cmp}^2}}{V_{iu}^2}.
\]

(18)

The mathematical relationship between the power and the capacitor voltage is calculated by

\[
\Delta p_{iu1} = C \cdot V_{cu1} \frac{dv_{cu1}}{dt} + \frac{2}{R} V_{cu1} \cdot \frac{v_{cu1}}{R}
\]

(19)

where \(R\) is the equivalent parallel resistance of dc capacitor. The transfer function is obtained by applying Laplace transformation to (18) and (19)

\[
G_{vh} = \frac{v_{cu1}}{\Delta e} = \frac{\sqrt{V_{iu}^2 - V_{cmp}^2}}{\sqrt{V_{iu}^2}} \cdot \frac{R \cdot L_c^2}{RCs + 2}.
\]

(20)

When the clustered dc voltage and the high-voltage dc link are regulated, the low-voltage dc link would be automatically maintained at the expected value because it is equal to the difference between the clustered dc voltage and the high-voltage dc link. According to (20), the individual voltage control algorithm is designed.
D. Design of DC Capacitor Voltages

In each phase cluster, the high-voltage converter and low-voltage converter complement each other to produce the sinusoidal command voltage. Therefore, the low-voltage dc link illustrated in Fig. 7 must be higher than the difference of sinusoidal command and quasi-square waveform to guarantee the safe operation. Taking u-phase cluster for an example, the constraint can be described as

\[
\begin{align*}
V_{cu1} < V_{i_u} < V_{cu1} + V_{cu2} \\
V_{x1} = V_{cu1} - V_{cmp} < V_{cu2} \\
V_{x2} = V_{cmp} < V_{cu2}
\end{align*}
\] (21)

where \(V_{cu1}\) is the high-voltage dc link, \(V_{cu2}\) is the low-voltage dc link, \(V_{i_u}\) is the magnitude of the sinusoidal command, and \(V_{cmp}\) is a constant threshold value. Inequality (21) could be rewritten as

\[
\begin{align*}
V_{cu1} < V_{i_u} < V_{cu1} + V_{cu2} \\
V_{cu1} < 2 \cdot V_{cu2} \\
V_{cu1} - V_{cu2} < V_{cmp} < V_{cu2}
\end{align*}
\] (22)

Based on (22), the reference value can be assigned as \(V_{cu1} = 110\) V, \(V_{cu2} = 65\) V, and \(V_{cmp} = 55\) V. This voltage ratio of \(V_{cu1} : V_{cu2}\) is close to 2:1, but there is a small margin of \(V_{cu1} - V_{cu2}/2 = 10\) V. This small margin is essential for individual voltage control. As a result, nine voltage levels of 0, \(\pm 45\), \(\pm 65\), \(\pm 110\), and \(\pm 175\) V are produced by each cluster. Although unequal steps exist, the output spectrum is still improved compared with the traditional five-level waveform.

IV. CONTROL STRATEGY

Fig. 8 shows a block diagram of the control algorithm proposed in this paper. The whole control algorithm consists of four parts, namely, decoupled current control, overall voltage control, clustered balancing control, and individual voltage control.

TABLE II

<table>
<thead>
<tr>
<th>Control Gains and Parameters</th>
<th>Symbols</th>
<th>Experiments</th>
<th>Symbols</th>
<th>Experiments</th>
</tr>
</thead>
<tbody>
<tr>
<td>(k_{ip})</td>
<td>0.1A/V</td>
<td>(k_{iq})</td>
<td>0.3A/V</td>
<td></td>
</tr>
<tr>
<td>(k_{ip})</td>
<td>25V/A</td>
<td>(k_{io})</td>
<td>166V/A</td>
<td></td>
</tr>
<tr>
<td>(k_{ip})</td>
<td>0.3A/V</td>
<td>(k_{iq})</td>
<td>1.5A/V</td>
<td></td>
</tr>
<tr>
<td>(k_{ip})</td>
<td>2V/A</td>
<td>(k_{io})</td>
<td>0.5A/V</td>
<td></td>
</tr>
</tbody>
</table>

A. Decoupled Current Control

Referring to Fig. 1, the set of voltage–current equation can be obtained as follows:

\[
\begin{align*}
L_{AC} \frac{di_{cu}}{dt} + R_L i_{cu} &= v_{sab} - v_{iu} \\
L_{AC} \frac{di_{cv}}{dt} + R_L i_{cv} &= v_{sbc} - v_{iv} \\
L_{AC} \frac{di_{cw}}{dt} + R_L i_{cw} &= v_{sca} - v_{iw}
\end{align*}
\] (23)

where \(R_L\) is the equivalent series resistance of the inductor. Applying the \(d-q\) transformations (23), the equations in \(d-q\) axis are derived

\[
\begin{align*}
L_{AC} \frac{di_d}{dt} - \omega L_{AC} \cdot i_q + R_L i_d &= v_{sd} - v_{id} \\
L_{AC} \frac{di_q}{dt} + \omega L_{AC} \cdot i_d + R_L i_q &= v_{sq} - v_{iq}
\end{align*}
\] (24)

The proportional and integral (PI) regulators with parameters of \(k_{ip}\) and \(k_{iq}\) are introduced for closed-loop current control. Parameters of \(k_{ip}\) and \(k_{iq}\) are given in Table II. The command voltages in \(d\)-axis and \(q\)-axis are given by

\[
\begin{align*}
v_{id} &= \omega L_{AC} \cdot i_q + v_{sd} - \left(k_{ip} + \frac{k_{iq}}{s}\right) (i^*_q - i_d) \\
v_{iq} &= -\omega L_{AC} \cdot i_d + v_{sq} - \left(k_{ip} + \frac{k_{iq}}{s}\right) (i^*_d - i_q)
\end{align*}
\] (25)

Here, \(i_d\) and \(i_q\) are the feedback currents in \(d\)-axis and \(q\)-axis, respectively. \(i^*_d\) and \(i^*_q\) are the \(d\)-axis and \(q\)-axis reference...
currents. The three-phase command voltages $v_{i_a^*}$, $v_{i_b^*}$, and $v_{i_c^*}$ can be obtained by applying the inverse $d$–$q$ transformations to $v_{id}$ and $v_{iq}$, as shown in Fig. 9.

The command current generating algorithm intended for detecting reactive and negative-sequence load current includes two parts: the reactive current algorithm and the negative-sequence current algorithm. These two parts are all based on $d$–$q$ transformations and moving average low-pass filter. The main difference between them is that the negative-sequence current algorithm needs to change the position of $b$-phase current and $c$-phase current when applying $d$–$q$ transformations. As shown in Fig. 10, the upper algorithm is for reactive current detection and the lower algorithm is for negative-sequence current detection. The three-phase line currents $i_{la}$, $i_{lb}$, $i_{lc}$ ought to be transformed into phase current because of the delta configuration of the three clusters. Fig. 11 shows the diagram for this transformation.

One of the solutions, as described in the following equation, is preferred because of its independence from the zero-sequence current [23]:

$$i_{uref} = -(i_{a}^* - i_{b}^*)/3$$
$$i_{uref} = -(i_{b}^* - i_{c}^*)/3$$
$$i_{uref} = -(i_{c}^* - i_{a}^*)/3.$$

(26)

B. Overall Voltage Control

Fig. 12 shows the overall voltage control diagram. $V_{dc_{ref}}$ is the reference value for the sum of all the dc capacitors’ voltage. $v_{dc_{sum}}$ acts as the feedback, which is obtained by summing up all the dc capacitors’ voltage. The PI regulator is preferred for overall control. The regulator design process for $k_{vp}$ and $k_{vi}$ is similar to that in the literature [24]. The output of PI regulator is the active component of command current.

C. Clustered Balancing Control

Fig. 13 shows the block diagram of clustered balancing control. Two PI regulators with constant parameters are adopted for calculating the amount of power for redistribution. The reference zero-sequence current is synthesized based on (1) and (6). Referring to (3) and (5), the closed-loop control is formed in Fig. 14, where $V_{cu}$ is the total dc voltage of u-phase cluster at steady-state operating point; $\tilde{v}_{cu}$ is the small voltage change around $V_{cu}$.

The closed-loop transfer function is obtained by

$$\frac{\tilde{v}_{cu}}{v_{dc_{ave}}} = \frac{Rk_{op}s + Rk_{oi}}{RCV_{cu}s^2 + (2V_{cu} + Rk_{op})s + Rk_{oi}}.$$ (27)

Based on (27), the parameters of $k_{op}$ and $k_{oi}$ for PI regulators are designed and the design processing can be found in the literature [24]. The parameters are given in Table II.
D. Individual Voltage Control

Fig. 15 shows the block diagram of the individual voltage control. Let $\Delta v_{cu1}$ be the difference between the reference voltage and the capacitor voltage of the high-voltage converter

$$
\Delta v_{cu1} = v_{cu1\_ref} - v_{cu1}.
$$

After introducing the proportional regulator $k_p$, the closed-loop control based on (20) is formed in Fig. 16, where $\dot{v}_{cu1}$ is the small voltage change around $V_{cu1}$.

The closed-loop transfer function is obtained by

$$
v_{cu1} \over v_{cu1\_ref} = \frac{R_k p C_{value} I_c^2}{2 R C V_{cu1} s + R C_{value} k_p I_c^2 + 4}.
$$

Based on (29), the regulator $k_p$ is designed and the design processing can be found in the literature [24].

V. EXPERIMENT RESULTS

Fig. 17 shows the experiment results verifying the effect of hybrid modulation. As the dc voltage of the high-voltage converter maintains at 110 V and those of the low-voltage converter stays at 65 V, nine-level voltage waveform is produced. The voltage steps of 45 and 65 V are close to each other, so it looks like a seven-level voltage waveform. The quasi-square-waveform voltage of the high-voltage converter and the three-level PWM-waveform voltage of the low-voltage converter are also generated as expected. This hybrid modulation scheme is effective in both producing high-quality low-harmonic output voltage and reducing the power loss of high-voltage converters.

Fig. 18 shows the experiment waveforms in capacitive operation at $q^* = -2.2$ kVA. At the beginning of the experiment, individual voltage control is not applied, while other controls remain active. The dc voltages of both the high-voltage converter and the low-voltage converter could not maintain at the given values. After a short time period of 20 s, the individual voltage control is enabled and the two dc voltage waveforms return to the given values quickly. Because the scope is limited to four channels, only the dc-link voltages of u-phase cluster and v-phase cluster are shown in Fig. 18(b). This experiment verifies that the individual voltage control is effective for regulating individual dc voltages.

Fig. 19 shows the experiment waveforms for testing clustered balancing control. At the beginning of the experiments, clustered balancing control is intentionally disabled while other controls are still enabled. The waveforms of dc voltages are shown clearly as four different curves in Fig. 19(b), and the dc voltages of three clusters are not maintained at the given values. After a short time period of 20 s, the clustered balancing control is triggered and the four curves converge as two quickly. The experiment verifies that the clustered balancing control is effective for balancing dc voltages among three clusters.
The dynamic performance of the hybrid multilevel STATCOM is also tested. Fig. 20 shows the experiment waveforms in a transient state from inductive to capacitive operation at 2.2 kVA. CH1: source voltage $v_{sa}$; CH2: output voltage $v_{sg}$; CH3: STATCOM phase current $i_{ca}$ (1 A/10 mV); CH4: reactive power $q^*$ (kVar/div).

Fig. 21 confirms the compensation effectiveness when the three-phase load is balanced. As shown in Fig. 21(a), the STATCOM system is enabled for 100 ms. During this interval, the $RL$ load is sufficiently compensated. After compensation, source-side current keeps in phase with source voltage. Fig. 21(b) shows that when the STATCOM system is in run mode, dc voltage is maintained at the given value and the fast response is ensured. Phases B and C have the same compensation effect, but only phase A curves are demonstrated due to the limitation of four channels of the scope.

Fig. 22 confirms the effect of unbalanced load compensation. As shown in Fig. 22(a), a great difference exists in the magnitudes of the STATCOM current. Because of the limitation of scope, only the currents of $i_{ca}$ and $i_{cb}$ are shown. During the compensating process, the dc mean voltage of capacitors stays at the reference value of 110 and 65 V, respectively in Fig. 22(b). The STATCOM output unbalanced line current to network for compensating unbalanced load, while a zero-sequence current is produced by the clustered balancing control algorithm for keeping the equal dc voltages of the three clusters. After compensation, the source-side currents have the same magnitude and keep in phase with the grid voltages, respectively, in Fig. 22(c). The power quality is greatly improved with the power factor being unit.

Fig. 23 confirms the effectiveness of dc voltage control when source voltage sag happens. As shown in Fig. 23, dc voltage keeps constant during the interval of source voltage sag, and the compensating current is not affected because of the source voltage sag.
Fig. 22. Experiment waveforms verifying the effect of compensating serious unbalance load. (a) CH1: source voltage $v_{sa}$; CH2: STATCOM line current $i_{ca}(1\text{ A/10 mV})$; CH3: source side current $i_{sa}(1\text{ A/10 mV})$; CH4: STATCOM line current $i_{cb}(1\text{ A/10 mV})$. (b) CH1: capacitor $v_{cu}$; CH2: capacitor voltage $v_{cu_{1}}$; CH3: STATCOM line current $i_{cb}(1\text{ A/10 mV})$; CH4: STATCOM line current $i_{cb}(1\text{ A/10 mV})$. (c) CH1: source voltage $v_{sa}$; CH2: source current $i_{sa}(1\text{ A/10 mV})$; CH3: source current $i_{sa}(1\text{ A/10 mV})$; CH4: STATCOM line current $i_{ca}(1\text{ A/10 mV})$.

Fig. 23. Experiment waveforms confirm the control effect when source voltage sag. CH1: source voltage $v_{sa}$; CH2: output voltage $v_{sa}$; CH3: capacitor $v_{cu}$; CH4: STATCOM line current $i_{ca}(1\text{ A/10 mV})$.

VI. CONCLUSION

This paper has analyzed the fundamentals of dc voltage control based on cascaded hybrid multilevel H-bridge converters. And then, a hybrid modulation for hybrid multilevel converter has been proposed and the control algorithm has also been designed in detail. The control scheme proposed in this paper is characterized by the capability of maintaining the unequal dc voltage at the given value without any additional circuit, as well as by the ability of compensating serious unbalanced load. This control strategy has taken full advantages of the available switching devices by operating the high-voltage device at low switching frequency and low-voltage device at high frequency. This control method along with the STATCOM system has the merits of producing high-quality output waveforms, reducing switching loss, and improving whole system’s efficiency. Experimental results obtained from a 100-V 3-kVA laboratory downscaled model have verified the effect of dc voltage control and dynamic performance of compensating seriously unbalancing load.

REFERENCES

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