An Improved Deadbeat Control for a Three-Phase Three-Line Active Power Filter with Current Tracking Errors Compensation

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Abstract—Active power filter (APF) plays an important role in compensating the harmonic component of a nonlinear load current. In this paper, Deadbeat Control (DBC), which has high control performance and fast dynamic response, is used as a current controller for an APF. An improved DBC (Imp_DBC) is introduced to suppress the adverse effect of the current sampling error and to enhance the interference rejection capability of the control system. The characteristics of the conventional DBC (Con_DBC) and Imp_DBC are analyzed using transfer functions in the discrete time domain. The robustness of system is improved with the inductance variation. Specifically, aiming at the dramatic change of harmonic component of the nonlinear load current, a current tracking error compensation (CTEC) method is proposed. The phenomena of the upper convex and lower concave in grid current are eliminated. Finally, the experimental setup of three-phase three-line APF is built and the effectiveness of this method is verified by experiments.

Index Terms—Active power filter, deadbeat control, sampling error, robustness, current tracking error

I. INTRODUCTION

In recent years, more and more power electronic equipment and other nonlinear loads are used in industrial due to the and civil applications; which causes harmonic pollution to become more serious and result in obvious degradation of power quality. Therefore, active power filter (APF) attracts increasing attention. This is a well-proven technology to suppress most of the load-current originated power quality problems [1-2].

Many current control methods for APF have been proposed. Hysteresis current control is adopted in [3], which has fast dynamic response, but the inverse relationship between the hysteresis threshold and the switching frequency will affect the control performance of the current. Repetitive control is used to track the harmonic component of the nonlinear load current in [4-5]. A dual-repetitive controller is used to improve the capability of current compensation in [4]. This has good performance on current tracking. However, the compensation capability is still insufficient because of the slow response of the repetitive controller in the special regions where the harmonic component of the nonlinear load current changes rapidly. A proportional integral (PI) regulator is also used to control the current [6-7]. In [6], different integral parameters are used for different frequency harmonic components of the nonlinear load current, making the design complex. To extract and track the different frequency harmonic components, a proportional resonant controller is applied in [8]. The harmonic component of the nonlinear load current cannot be compensated totally. Moreover, it needs several fundamental cycles to reach steady state.

Adaptive linear neuron and feed-forward multilayer neural network techniques are used to compensate the harmonic component of the nonlinear load current [9]. Harmonic detection of the nonlinear load current is a key technique, which has an important effect on both accuracy and response of the APF [10-13]. The harmonic component of the nonlinear load current as the reference current must be reliable and accurate. Predictive and adaptive artificial neural network (ANN) algorithms are used for APF in [10]. This method is derived from an ANN-based PI controller and the dynamic process cannot be ensured. In [11], a digital filter is used for fast harmonic component detection with a complex algorithm but it is difficult to achieve good steady state harmonic tracking performance. A deadbeat control (DBC) scheme is suitable in current control of APF because of the advantages of high control accuracy and fast dynamic response [14-15].

As is well known, control delay exists in all digital controls. DBC also has such a problem, which must be considered. The impact of control delay on current is analyzed quantitatively in [16]. To solve this problem, many advanced techniques have been proposed. A one-step prediction method is adopted to track current in [14, 17]. An improved Smith predictive compensator is established to compensate control delay and better performance can be obtained [18]. However, a Smith compensator is still a one-step prediction. In [19], a time delay compensator is proposed. Although it can reduce the impact of control delay, this method needs higher current sample accuracy.

Besides the problem raised by the control delay, the current tracking error cannot be neglected in APF, especially in the regions where the harmonic component of the nonlinear load current changes rapidly. In [5], a repetitive controller that is based on regeneration spectrum and sensitivity function is adopted to weaken the error in steady state; showing the drawback of slow dynamic response. A dual repetitive controller is proposed to compensate the harmonic component of the nonlinear load current in [4]. However, the phenomena of upper convex and lower concave current cannot be eliminated.
completely and the capability of the harmonic compensation is insufficient in the special regions. The phenomena are also obvious in grid current [12, 20]. In addition, the filter inductance cannot be measured. A difference between the nominal inductance and the actual inductance is unavoidable, which is the factor that affects the control performance of the current. In [17, 21], the stability limitation of the deadbeat current control is presented. In [22], a wide bandwidth impedance identification method is used in a deadbeat current controller for a grid-connected inverter, which can reduce the influence of the inductance variation. An improved predictive current control algorithm is proposed to enhance the robustness [23].

In this paper, an improved DBC (Imp_DBC) with current tracking error compensation (CTEC) is introduced for APF. Section II describes the model of the APF in the two phase stationary frame. The conventional DBC (Con_DBC) with two-step prediction is introduced and Imp_DBC is proposed in Section III. Then, more detailed analyses for Con_DBC and Imp_DBC are discussed in Section IV. Analysis of response to current sampling error of Con_DBC and Imp_DBC is given in Section V. CTEC is presented in Section VI; which is used to eliminate the phenomena of upper convex and lower concave current. In Section VII, the design of control system based Imp_DBC with CTEC is presented and the dynamic process is analyzed. In Section VIII, the experimental setups of APF are built and the effectiveness of the proposed method is verified experimentally. Conclusions are drawn in Section IX.

II. MODEL OF APF

The topology of a three-phase three-line APF is shown in Fig. 1. Here $u_z$ is the output voltage of phase $z$, $i_z$ is the current of phase $z$ injected from the APF to the grid (which is used to compensate the harmonic component of the nonlinear load), and $i_{dc}$ is the current of the dc bus. As an example, the nonlinear load is an uncontrollable rectifier with a resistive-inductive load. $i_{in}$ is the input current of uncontrollable rectifier and includes fundamental current component $i_{ref}$ and harmonic component current $i_{h}$. In the ABC stationary frame, the continuous time model of APF can be expressed as:

$$u_z = e_z + R_i i_z + L_i \frac{di_z}{dt} \tag{1}$$

The Clarke transformation is used in the following discussion. $X^{abc}$ is the column vector in the stationary $abc$ reference frame, and $X^{\alpha\beta}$ is the column vector in the $ABC$ stationary frame. The matrix $C_{3s/2s}$ is the transformation matrix from $ABC$ to $\alpha\beta$, which is expressed as:

$$C_{3s/2s} = \begin{bmatrix} \frac{2}{3} & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}$$

(2)

Ignoring $R_i$ due to its relative small value, the continuous time model of APF in the stationary $\alpha\beta$ reference frame can be expressed as:

$$u_{\alpha\beta} = e_{\alpha\beta} + L_i \frac{di_{\alpha\beta}}{dt} \tag{3}$$

III. CON_DBC AND IMP_DBC

A. Con_DBC

In the stationary $\alpha\beta$ reference frame, the differential equation of the grid-side current can be derived by the continuous time model of the APF given by (3); which can be expressed as:

$$\frac{di_{\alpha\beta}}{dt} = \frac{u_{\alpha\beta} - e_{\alpha\beta}}{L_i} \tag{4}$$

In this paper, $y(n)$, $y(n-1)$ and $y(n+1)$ denote the value in the present cycle, last cycle and next cycle, respectively. The symbols $\scriptstyle \hat{y}$, $\hat{\scriptstyle y}$, $\tilde{y}$ denote the sampled value or real value, reference value, predictive value, estimated value and calibrated value, respectively.

The differential equation of the grid-side current can be discretized by using backward difference method, allowing (4) to be rewritten as:

$$i_{\alpha\beta}(n+1) - i_{\alpha\beta}(n) = \frac{u_{\alpha\beta}(n+1) - e_{\alpha\beta}(n+1)}{T_i} L_i \tag{5}$$

where $T_i$ is the control cycle, and (5) can be simplified further as:

$$i_{\alpha\beta}(n+1) = i_{\alpha\beta}(n) + \frac{T_i}{L_i} \left[ u_{\alpha\beta}(n+1) - e_{\alpha\beta}(n+1) \right]$$

$$= i_{\alpha\beta}(n) + \frac{T_i}{L_i} \Delta u_{\alpha\beta}(n+1) \tag{6}$$

where $\Delta u_{\alpha\beta}(n+1)$ represents the voltage increment vector, which can be expressed as:

$$\Delta u_{\alpha\beta}(n+1) = u_{\alpha\beta}(n+1) - e_{\alpha\beta}(n+1) \tag{7}$$

The oversampling technique is used as a software antialiasing filter [24, 25], as shown in Fig. 2 (a). The current is sampled four times in one control cycle and the average value is regarded as the sampled value in this cycle.

Because the data sample, process, and execution are parallel in different function modules of digital signal processor (DSP), it should be noted that there are two step control delays from sample to execution in DSP. The data which is sampled in the present control cycle will be used to calculate control variables in the next control cycle; this is the first step control delay. The calculation results of control variables in the present control cycle will be executed in the next control cycle; this is the second step control delay. The two-step control delays can be seen in Fig. 2(b).

A two-step prediction method has been proposed in [26-27]. This prediction method is used to improve the current control performance in this paper. The first prediction step is to

![Fig. 1. Topology of three-phase three-line APF.](image-url)
calculate $\Delta \mathbf{u}_{ap}(n+1)$, which will be executed in the next control cycle (but should be calculated in the present control cycle). Based on the current vector $\mathbf{i}_{ap}(n)$ and the reference current vector $\hat{\mathbf{i}}_{ap}(n)$, $\Delta \mathbf{u}_{ap}(n+1)$ can be calculated as:

$$\Delta \mathbf{u}_{ap}(n+1) = \frac{L_c}{T_c}[\hat{\mathbf{i}}_{ap}(n+1) - \mathbf{i}_{ap}(n)] \quad (8)$$

To calculate $\Delta \mathbf{u}_{ap}(n+1)$, the current vector $\mathbf{i}_{ap}(n)$ is needed but it is being sampled in the present control cycle and so the second prediction is needed. $\hat{\mathbf{i}}_{ap}(n)$ should be predicted based on $\mathbf{i}_{ap}(n-1)$ and $\Delta \mathbf{u}_{ap}(n)$. This prediction can be expressed as:

$$\hat{\mathbf{i}}_{ap}(n) = \mathbf{i}_{ap}(n-1) + \frac{T_c}{L_c} \Delta \mathbf{u}_{ap}(n) \quad (9)$$

Substituting (9) into (8), $\Delta \mathbf{u}_{ap}(n+1)$, based on two-step prediction method, can be calculated as:

$$\Delta \mathbf{u}_{ap}(n+1) = \frac{L_c}{T_c}[\hat{\mathbf{i}}_{ap}(n+1) - \mathbf{i}_{ap}(n-1)] - \Delta \mathbf{u}_{ap}(n) \quad (10)$$

If switching frequency is much higher than grid frequency, $\hat{\mathbf{e}}_{ap}(n+1)$ and $\hat{\mathbf{e}}_{ap}(n)$ can be predicted by $\mathbf{e}_{ap}(n-1)$ through the rotation transformation. This prediction can be expressed as:

$$\begin{align*}
\hat{\mathbf{e}}_{ap}(n+1) &= \mathbf{e}_{ap}(n-1) e^{j2\omega_0 T_c} , \\
\hat{\mathbf{e}}_{ap}(n) &= \mathbf{e}_{ap}(n-1) e^{j\omega_0 T_c} ,
\end{align*}$$

(11)

where $e^{j2\omega_0 T_c}$ and $e^{j\omega_0 T_c}$ are rotation transformation factor. At last, the output voltage vector of APF in the next control cycle can be expressed as:

$$\mathbf{u}_{ap}(n+1) = \frac{L_c}{T_c}[\hat{\mathbf{i}}_{ap}(n+1) - \mathbf{i}_{ap}(n-1)] - [\mathbf{u}_{ap}(n) - \hat{\mathbf{e}}_{ap}(n)] + \hat{\mathbf{e}}_{ap}(n+1) \quad (12)$$

$$\Delta \mathbf{u}_{ap}(n+1)$$ can be predicted by (11), which will be executed in the next control cycle. The performance of DBC depends on the accuracy of the model parameters [17]. However, the inductance between the
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APF and grid cannot be accurately measured. A difference between the nominal inductance \( L_{\text{nom}} \), which is used in the DBC, and the actual inductance \( L_s \) is unavoidable. The inductance variation coefficient \( k_L \) can be expressed as:

\[
k_L = \frac{L_{\text{nom}}}{L_s}
\]  

(16)

The control structure of Con_DBC is shown in Fig. 4. In Fig.4, \( G_{z}(z) \) represents the transfer function of Con_DBC in the \( z \)-domain given by (17), which is used to calculate the output voltage in the next cycle. It can be expressed as:

\[
G(z) = k_L \frac{L_s T_s}{L_s z^2 - 1}
\]  

(17)

\( G_{z}(z) = z^2 \) represents the two-step control delay. According to equation (10), the voltage increment vector \( \Delta u \) in the \( (n-1) \)th cycle can be derived. Based on that, \( G(z) = 1 + z^{-1} \), \( G_{z}(z) = T_s / L_s \), and \( G_{z}(z) = 1/(1-z^{-2}) \) can be obtained. The product of \( G(z) \) and \( G_{z}(z) \) represent the discrete model of the APF, which can be expressed as:

\[
G_{\text{con}}(z) = z^2 - 1 + k_L
\]

(18)

Then, the closed loop transfer function of Con_DBC can be derived from Fig. 4 as:

\[
G_{\text{con}}(z) = \frac{G_{z}(z) - 1}{1 + G_{z}(z) - 1 + k_L}
\]  

(19)

It follows that the characteristic equation of closed loop transfer function is given by:

\[
D_{\text{con}}(z) = z^2 - 1 + k_L = 0
\]

(20)

According to Jury’s stability criterion in the discrete time domain, the constraint condition of \( k_L \) can be expressed as:

\[
0 < k_L < 2
\]  

(21)

As is well known, if all system closed loop poles are located in the unit circle, the system is stable. Fig. 5 plots the closed loop poles of Con_DBC when \( k_L \) varies from 0.5 to 2. As can be seen, when \( k_L \) is less than 2, the system is always stable. When \( k_L \) reaches 2, the system closed loop poles are located on the boundary of the unit circle. Thus, the upper limit of \( k_L \) is 2 in Con_DBC, which is identical to the result in [17].

![Fig. 5. Closed loop poles of Con_DBC with different inductance variation coefficients.](image)

B. Analysis of Imp_DBC

Combining (13), (14) and (15) the control structure of Imp_DBC can be derived, as shown in Fig. 6.

The closed loop transfer function of Imp_DBC can be expressed as:

\[
G_{\text{imp}}(z) = \frac{k_L z - k_L k_g}{z^2 - k_g z^2 + (k_L + k_g - k_L)z}
\]

(22)

The characteristic equation of the closed loop transfer function is given by:

\[
D_{\text{imp}}(z) = z^2 - k_g z^2 + (k_L + k_g - k_L)z = 0
\]

(23)

By using Jury’s stability criterion, the relationship between \( k_L \) and \( k_g \) can be derived as:

\[
0 < k_L < 2 - \frac{k_g}{1 - k_L}
\]

(24)

From (24), the range of the inductance variation coefficient \( k_L \) is determined by the weight coefficient \( k_g \). Due to \( 0 < k_g < 1 \), the upper limit of \( k_L \) is greater than 2 in Imp_DBC. Therefore, Imp_DBC can enhance the system robustness. Based on the transfer function \( G_{\text{imp}}(z) \), Fig. 7 shows the closed loop poles of Imp_DBC. When \( k_L = 1.7 \), Fig. 7(a) shows all closed loop poles when the weight coefficient \( k_g \) varies from 0 to 1.1. From Section IV.A, the stability of the system under Con_DBC can be met. Under Imp_DBC, it is clear that when \( k_L \) is close to 1,
In fact, considering the reliability of the nominal inductance $L_{sm}$, it can be seen that all the poles are located within the unit circle. The frequency characteristic curves of $Con_DBC$ and $Imp_DBC$ overlap when the frequency is less than 100Hz, but the cutoff frequency of $Imp_DBC$ is higher than that of $Con_DBC$ which indicates that $Imp_DBC$ has faster transient response.

V. ANALYSIS OF RESPONSE TO CURRENT SAMPLING ERROR OF $Con_DBC$ AND $Imp_DBC$

The control structure of $Con_DBC$ with the current sampling error perturbation is shown in Fig. 9(a). $D(z)$ represents the interference of current sampling error. The interference of current sampling error can be equivalent to interference output of voltage increments; which will be discussed in Section VI.A. The closed-loop transfer function of current error can be expressed as:

$$G_{D_{con}}(z) = \frac{z^2G_3(z)G_5(z)}{1 + G_3(z)z^2G_4(z)G_4(z)} \left(1 + k_L z^{-1}\right)$$  \hspace{1cm} (25)

The control structure of $Imp_DBC$ with the current error perturbation is shown in Fig. 9(b). The closed-loop transfer function of current error can be expressed as:

$$G_{D_{impc}}(z) = \frac{z + 1}{L_z z^{-1} - k_{fc}}$$  \hspace{1cm} (26)

The current sampling error can be considered as a unit impulse sampling error. The response of a unit impulse sampling error with different $k_{fc}$ can be found in Figs. 10 and 11.

The comparison of different $k_{fc}$ values is shown in Fig.10 with $k_{fc}=1.8$. When $k_{fc}=0.9$ the maximum oscillation amplitude is about 0.95, but the time to recover to steady state is long (almost 0.15s), as shown in Fig. 10(a). When $k_{fc}=0.5$, the maximum oscillation amplitude is about 1.3 and it needs about 0.1s to recover to steady state, as shown in Fig.10 (b). When $k_{fc}=0.3$, the maximum oscillation amplitude is about 1.5 and it needs approximately 0.13s to recover to steady state and it oscillates several times, as shown in Fig.10 (c). When $k_{fc}$ is set to 1.4, the comparison of the different $k_{fc}$ is shown in Fig.11. Similar results can be seen.

with Fig. 7, it can be seen that the robustness of the system is enhanced under $Imp_DBC$. The Bode diagram of the closed loop transfer function of $Con_DBC$ and $Imp_DBC$ is shown in Fig. 8. Here, $k_L$ is set to 0.5 and $k_{fc}$ is set to 1.5. As can be seen from the diagram, the frequency characteristic curves of $Con_DBC$ and $Imp_DBC$ overlap when the frequency is less than 100Hz, but the cutoff frequency of $Imp_DBC$ is higher than that of $Con_DBC$ which indicates that $Imp_DBC$ has faster transient response.
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needed. As

Con_DBC.

control performance under Imp_DBC is improved over Con_DBC is much greater than that under Imp_DBC. So the much longer than that under Imp_DBC and the overshoot under

the present cycle can be expressed as:

Fig. 11. Comparison of the unit impulse response of different current weight coefficients, \( k_c = 1.4 \) (a) \( k_b = 0.9 \) (b) \( k_b = 0.5 \) (c) \( k_b = 0.3 \).

The unit step responses of Con_DBC and Imp_DBC are presented in Fig. 12. When \( k_c \) is set to 0.5, \( k_b = 1.4 \) and 0.6 are chosen as examples. The response time under Con_DBC is much longer than that under Imp_DBC and the overshoot under Con_DBC is much greater than that under Imp_DBC. So the control performance under Imp_DBC is improved over Con_DBC.

When \( k_b \) is changed, in order to get better control performance, adjustments should be made with \( k_b \). Selecting a larger \( k_b \) allows larger inductance deviation and better robustness is achieved. Nevertheless, the current response time is longer and the superiority of DBC would be lost partly.

VI. CURRENT TRACKING ERROR COMPENSATION

A. Analysis of tracking error

To calculate \( \Delta u_{\text{opt}}(n+1) \) in (8), the current vector \( i_{\text{opt}}(n) \) is needed. As \( i_{\text{opt}}(n) \) is being sampled in the present cycle, \( i_{\text{opt}}(n) \) must be predicted based on \( i_{\text{opt}}(n-1) \) and \( \Delta u_{\text{opt}}(n) \). The difference between \( i_{\text{opt}}(n) \) and \( i_{\text{opt}}(n) \) results in current tracking error. The current tracking error is predominant in the region where the harmonic component of the nonlinear load current changes rapidly, as shown in Fig. 13. In this section, the current tracking error is analyzed and a handling method is proposed. According to (10), \( \Delta u_{\text{opt}}(n) \) in the present cycle can be expressed as:

\[
\Delta u_{\text{opt}}(n) = \frac{I_s}{T_s} \left[ i_{\text{opt}}(n) - i_{\text{opt}}(n-2) \right] - \Delta u_{\text{opt}}(n-1) \tag{27}
\]

Substituting (27) into (10), then (10) can be rewritten as:

\[
\Delta u_{\text{opt}}(n+1) = \frac{I_s}{T_s} \left[ i_{\text{opt}}(n+1) - i_{\text{opt}}(n-1) - i_{\text{opt}}(n) + i_{\text{opt}}(n-2) \right]
+ \Delta u_{\text{opt}}(n-1) \tag{28}
\]

According to the derivation procedure of (28), \( \Delta u_{\text{opt}}(n+1) \) can be recurred to the \((n-k)\)th cycle. It can be expressed as:

\[
\Delta u_{\text{opt}}(n+1) = \frac{I_s}{T_s} \left[ i_{\text{opt}}(n+1) - i_{\text{opt}}(n-1) \right] - \Delta u_{\text{opt}}(n)
= \frac{I_s}{T_s} \left[ i_{\text{opt}}(n+1) - i_{\text{opt}}(n) \right] 
+ \sum_{k=1}^{n} (-1)^k \times L_s \frac{\Delta u_{\text{opt}}(n-k+1)}{T_s} 
+ (-1)^k \left[ L_s \left[ i_{\text{opt}}(n-k-1) - i_{\text{opt}}(n-k) \right] \right] - \Delta u_{\text{opt}}(n-k-1) \tag{29}
\]

In the right side of (29), the first term is the voltage increment in the next cycle, which is calculated by using the reference current vectors \( i_{\text{opt}}(n+1) \) and \( i_{\text{opt}}(n) \). The second term is the cumulative voltage increment caused by the current error. The third term is the voltage increment in the \((n-k)\)th cycle. It is important to note that \( k \) starts at two.

In (29), The current tracking error \( \Delta i_{\text{opt}}(n-k+1) \) in the \((n-k+1)\)th cycle can be expressed as:

\[
\Delta i_{\text{opt}}(n-k+1) = i_{\text{opt}}(n-k+1) - i_{\text{opt}}(n-k+1) \tag{30}
\]

Fig. 12. Comparison of the unit step response of the Con_DBC and Imp_DBC, (a) \( k_c = 1.4 \) and \( k_b = 0.5 \); (b) \( k_c = 0.6 \) and \( k_b = 0.5 \).

Fig. 13. Impact of current tracking error on grid current.

Fig. 14. Typical harmonic component of the nonlinear load current. (a) The nonlinear load current. (b) The harmonic component. (c) The partial extension of harmonic component.
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Fig. 15. Flow chart of the CTEC algorithm.

Fig. 16. Dynamic experimental results of Imp_DBC. (a) Dynamic experimental result. (b) Expansion of (a).

B. CTEC

A typical nonlinear load current is taken as an example to explain the implementation of CTEC, as shown in Fig. 14(a). Fig. 14(b) shows the harmonic component of the nonlinear load current. As can be seen, in the regions where the harmonic component changes slowly, the APF can well compensate the harmonic component of the nonlinear load current. At this moment, the impact of the tracking error can be ignored. However, in the regions where the harmonic component changes rapidly as shown in Fig. 14(c), the impact of the tracking error cannot be ignored because of the cumulative voltage increment.

This leads to the reason of the poor current tracking performance in Fig. 13 which is caused by the cumulative voltage increment. In the rising and decreasing regions of the grid current, the cumulative voltage increment will result in upper convex and lower concave grid current, respectively. Similar experimental results can be referred to [12, 14 and 16].

In order to reduce the influence of the current tracking error in the region where the harmonic component changes rapidly, CTEC is proposed by the analysis in Section VI.A. From (29), the cumulative voltage increment vector \( \Delta u^{\text{comp}} \) can be expressed as:

\[
\Delta u^{\text{comp}} = \sum_{k=1}^{n} (-1)^{k+1} \times \frac{L}{T_s} \Delta i^{\text{ref}}(n-k)
\]

Subtracting \( \Delta u^{\text{comp}} \) from \( u^{\text{ref}}(n+1) \), the output voltage vector of APF in the next control cycle can be expressed as:

\[
u^{\text{ref}}(n+1) = \frac{L}{T_s} \left[ i^{\text{ref}}(n+1) - i^{\text{ref}}(n-1) \right] - \Delta u^{\text{comp}}
\]

Comparing (15) with (32), it can be seen that the current tracking error can be eliminated when \( \Delta u^{\text{comp}} \) is added. However, one problem still needs to be solved: how to determine the value of \( k \) in (31). A CTEC criterion is adopted, which can solve this problem effectively. Once the harmonic component enters the region with rapid change as shown in Fig. 14(c), \( k \) is counted from one until the harmonic component exits this special region. If the region includes \( j \) control cycles, \( k \) counts from one to \( j \). Once the harmonic component exits the region, \( \Delta u^{\text{comp}} \) is set to zero immediately. Thus, \( k \) is determined and the cumulative voltage increment vector \( \Delta u^{\text{comp}} \) is determined as well.

The flow chart of the current tracking error compensation algorithm is presented in Fig. 15. The calculation of the cumulative voltage increment is triggered when the difference between the reference current \( i^{\text{ref}}(n+1) \) and \( i^{\text{ref}}(n) \) is more than the predetermined value. How to obtain the predetermined value will be discussed next.

Fig. 16 presents the dynamic experimental results of Imp_DBC, which is mainly to present the response time of Imp_DBC when the reference current changes suddenly. The amplitude of the reference current changes from 20A to 30A and from Fig. 16 (b), the response time of Imp_DBC is about 230\( \mu \)s. In the experiment, the switching frequency is 9k Hz,
meaning the response time of Imp_DBC is about two control cycles.

The control diagram of Imp_DBC with CTEC is shown in Fig. 17. The following steps achieve Imp_DBC with CTEC:

**Step I:** One-step prediction is completed with (13), and then the predictive current \( \bar{i}_{\text{Δ}}(n-1) \) can be obtained.

**Step II:** The current \( i_{\text{Δ}}(n-1) \) in the \((n-1)\)th cycle is calculated by using \( \bar{i}_{\text{Δ}}(n-1) \) and \( i_{\text{Δ}}(n-1) \), as shown in (14).

**Step III:** Determine \( k \) in (29) by using the current tracking error compensation criterion. Then, calculate the cumulative voltage increment vector \( \Delta u_{\text{comp}} \), as shown in (31). This step is a key step for CTEC.

**Step IV:** Complete two-step prediction. Calculate the output voltage vector \( u_{\text{comp}}(n+1) \) in the \((n+1)\)th cycle, as shown in (32).

In order to describe the detailed operation procedure of CTEC, the harmonic component in Fig. 14(c) is taken as an example. \( i'(n-k) \) represents the reference harmonic current in the \((n-k)\)th cycle. For example, the harmonic component has entered the region with rapid change for \( j \) control cycles, which means that \( k = j+1 \). As \( j = 3 \), the cumulative voltage increment vector \( \Delta u_{\text{comp}} \) can be expressed as:

\[
\Delta u_{\text{comp}} = \sum_{k=1}^{3} (-1)^{k+1} \frac{L}{T_s} \Delta i(n-k)
\]

(33)

In the next cycle, if the region with rapid change is over, \( \Delta u_{\text{comp}} \) is set to 0 again.

**VII. DESIGN OF THE CONTROL SYSTEM**

**A. Design of the Control System**

The control diagram of Imp_DBC with CTEC for APF is presented in Fig. 18. The harmonic component detection method of the nonlinear load current can be referred to [9]. The dc bus voltage of APF is sampled and a low-pass filter (LPF) is used to eliminate the ripple. A proportional integral regulator is adopted in the outer loop to calculate active power reference \( p' \). On the basis of instantaneous power theory, the fundamental reference current \( i_{\text{ref}}(n+1) \) can be obtained. The reference harmonic component \( i_{h}(n+1) \) can be detected from the nonlinear load current. Then \( i_{\text{in}}(n+1) \) and \( i_{\text{hp}}(n+1) \) are added as the total reference current \( i_{\text{ref}}(n+1) \) in the next cycle.

Imp_DBC with CTEC is used as current controller to improve the current control performance of APF. The actual three phase current outputted by APF is sampled and the current vector \( i_{\text{ref}}(n-1) \) can be obtained by using the Clarke transformation. Next, the output voltage \( u_{\text{comp}}(n+1) \) can be calculated by using the Imp_DBC with CTEC. The detailed process can be found in Section VIB. Finally, the three-phase modulation voltage \( u_{\text{abc}} \) can be obtained by using the inverse Clarke transformation.

**B. Dynamic Process Analysis**

When the nonlinear load current changes suddenly, the harmonic component changes suddenly as well. The time delay of the harmonic detection is unavoidable and will weaken the compensation performance of the APF during the dynamic process. Prior knowledge must be used to reconstruct reference harmonic component of nonlinear load current immediately while the transient happens. The prior knowledge is that only the amplitude of the harmonic component changes when the nonlinear load current changes suddenly. The changing coefficient can be expressed as:

\[
k = \frac{\Delta u_{\text{ref}}(n-1)}{\Delta u_{\text{ref}}(n-1)}
\]

(34)

where \( \Delta u_{\text{ref}}(n-1) \) represents the nonlinear load current in the last control cycle and \( \Delta u_{\text{ref}}(n-1) \) is the nonlinear load current in the last fundamental period. \( \Delta u_{\text{ref}}(n-1) \) and \( \Delta u_{\text{ref}}(n-1) \) are corresponding to the same phase angle of grid. The reference harmonic components of the nonlinear load current can be reconstructed as:

\[
\begin{align*}
\Delta i_{\text{ref}}(n+1) &= k_{\alpha} \Delta i_{\text{ref}}(n+1) \\
\Delta i_{\text{ref}}(n+1) &= k_{\beta} \Delta i_{\text{ref}}(n+1)
\end{align*}
\]

(35)

where \( \Delta i_{\text{ref}}(n+1) \) represents the reconstructed reference harmonic component after the nonlinear load current changes. From this, the compensation performance of APF during the dynamic process can be improved.

**VIII. EXPERIMENTAL RESULTS**

To verify the effectiveness of the control strategy proposed in this paper, a prototype of three-phase three-line APF is built, as shown in Fig. 19. The DSP MC56F8345 manufactured by Freescale is used as the main control chip and the switch device is the IGBT CM150DX-24S-E. The nonlinear load is used as the harmonic source composed of an uncontrollable rectifier with resistance-inductance (RL) load. The system parameters are listed in Table I.

![Experimental setup. (a) three-phase three-line APF; (b) uncontrollable rectifier with inductance-resistance load](image)

Table I

<table>
<thead>
<tr>
<th>Parameters of APF and Harmonic Load</th>
<th>Table 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance (μF)</td>
<td>6600</td>
</tr>
<tr>
<td>DC bus voltage (V)</td>
<td>720</td>
</tr>
<tr>
<td>Line voltage of grid (V)</td>
<td>380</td>
</tr>
<tr>
<td>Three-phase three-line APF</td>
<td></td>
</tr>
<tr>
<td>Switching Frequency (Hz)</td>
<td>9000</td>
</tr>
<tr>
<td>Filter inductance (mH)</td>
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</tr>
<tr>
<td>Resistance (Ω)</td>
<td>18</td>
</tr>
<tr>
<td>Inductance (mH)</td>
<td>1</td>
</tr>
</tbody>
</table>

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A. Verification of Imp_DBC

Fig. 20 shows the experimental results of Con_DBC and Imp_DBC in the steady-state. The reference current, actual current, and the steady-state error of current are shown. As can be seen from Fig. 20(a), the current sampling error may appear at region A. Under Con_DBC, the envelope of the current is thick without the action of the current correction algorithm. The steady-state error fluctuates with high frequency. On the contrary, the envelope of the current is thin under Imp_DBC in Fig. 20(b). There is no high frequency fluctuation in the steady-state error. Due to the effect of the built-in low pass action, the steady-state error fluctuates at grid frequency under Imp_DBC but the amplitude of the fluctuation is very small and can be ignored. Although Imp_DBC loses some deadbeat behavior because of the built-in low pass action, a better control performance of the current can be obtained.

B. Verification of Harmonic Compensation

The phase current of nonlinear load and its harmonic component are shown in Fig. 21(a). The total harmonic distortion (THD) and spectrum of phase current of nonlinear load are given in Fig. 21(b). Fig. 22(a) shows the experimental results under Con_DBC. As can be seen, there are upper convexities and lower concavities on the grid current. Moreover, there are some regions with a thick envelope on the grid current, which is caused by the random sample error. Fig. 22(b) shows the experimental results under Imp_DBC. Notably, there are still obvious upper convex and lower concave regions on the grid current. However, the envelope of the grid current is thinner than that under Con_DBC. The effectiveness of Imp_DBC to suppress adverse effect due to the random sample error is verified.

Fig. 22(c) shows the experimental results under Con_DBC with CTEC. There is no upper convexity or lower concavity on the grid current. However, there are some regions with thick envelope on the grid current, which is caused by the random sample error. Fig. 22(d) shows the experimental results under Imp_DBC with CTEC. Again, there is no upper convex or lower concave regions on the grid current and furthermore, the envelope is thinner than that under Con_DBC with CTEC.

When the APF is used, the idiographic data of harmonic of grid current under different control method is listed in Table II. It can be seen that the THD of the grid current is 10.9%, 6.16%, 5.7% and 2.67% under Con_DBC, Imp_DBC, Con_DBC with CTEC and Imp_DBC with CECT, respectively. When the nonlinear load current changes suddenly, the dynamic experimental results under Con_DBC and Imp_DBC with CTEC are given in Fig. 23. A nice compensation performance can be achieved during the dynamic process. The response time of current tracking is about 5ms. With the dynamic experimental results, the applicability of the assumption made in Section VII.B is verified. In addition, Imp_DBC with CTEC is effective during the dynamic process.

IX. CONCLUSIONS

To mitigate the adverse effect due to the random sample error, an improved DBC is proposed for a three-phase three-line APF in this paper. The proposed method can improve current control performance and enhance the interference suppression ability. The robustness of system is also enhanced under the improved DBC compared with the conventional DBC. The current tracking error in the conventional DBC is analyzed. Aiming at the tracking error, a CTEC method is proposed. The proposed CTEC method can eliminate the upper convex and lower concave current in the special regions where the harmonic component of the nonlinear load current, which should be compensated by the APF, changes rapidly. The harmonic compensation performance of the APF is improved. The effectiveness of this method is verified experimentally.
Fig. 22. Steady state experimental results under different control method. (a) Con_DBC; (b) Imp_DBC; (c) Con_DBC with CTEC; (d) Imp_DBC with CTEC.
Fig. 23. Dynamic experimental results under different control method. (a) Con_DBC; (b) Imp_DBC with CTEC.

REFERENCES


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